

FIG. 1

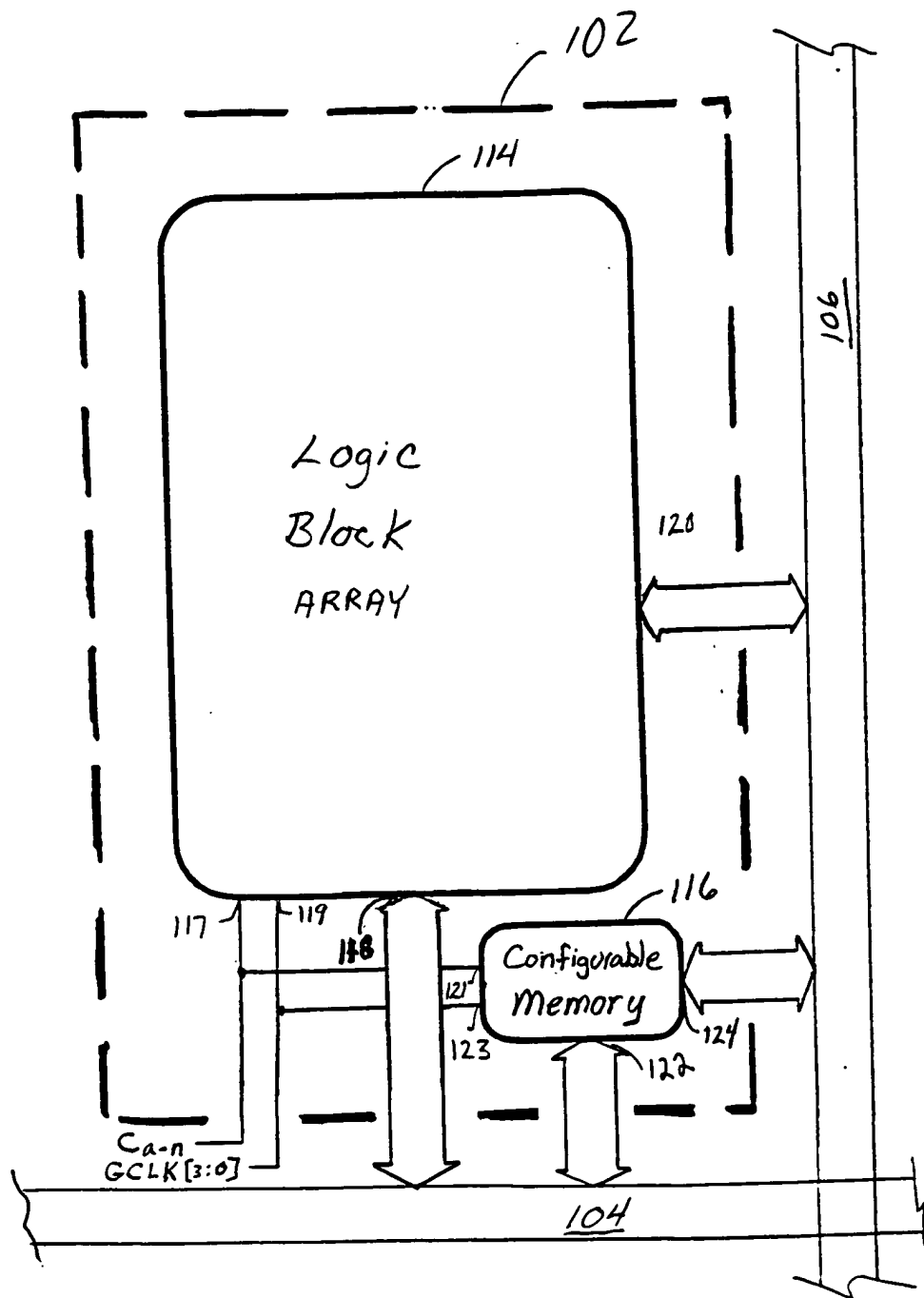


FIG.2

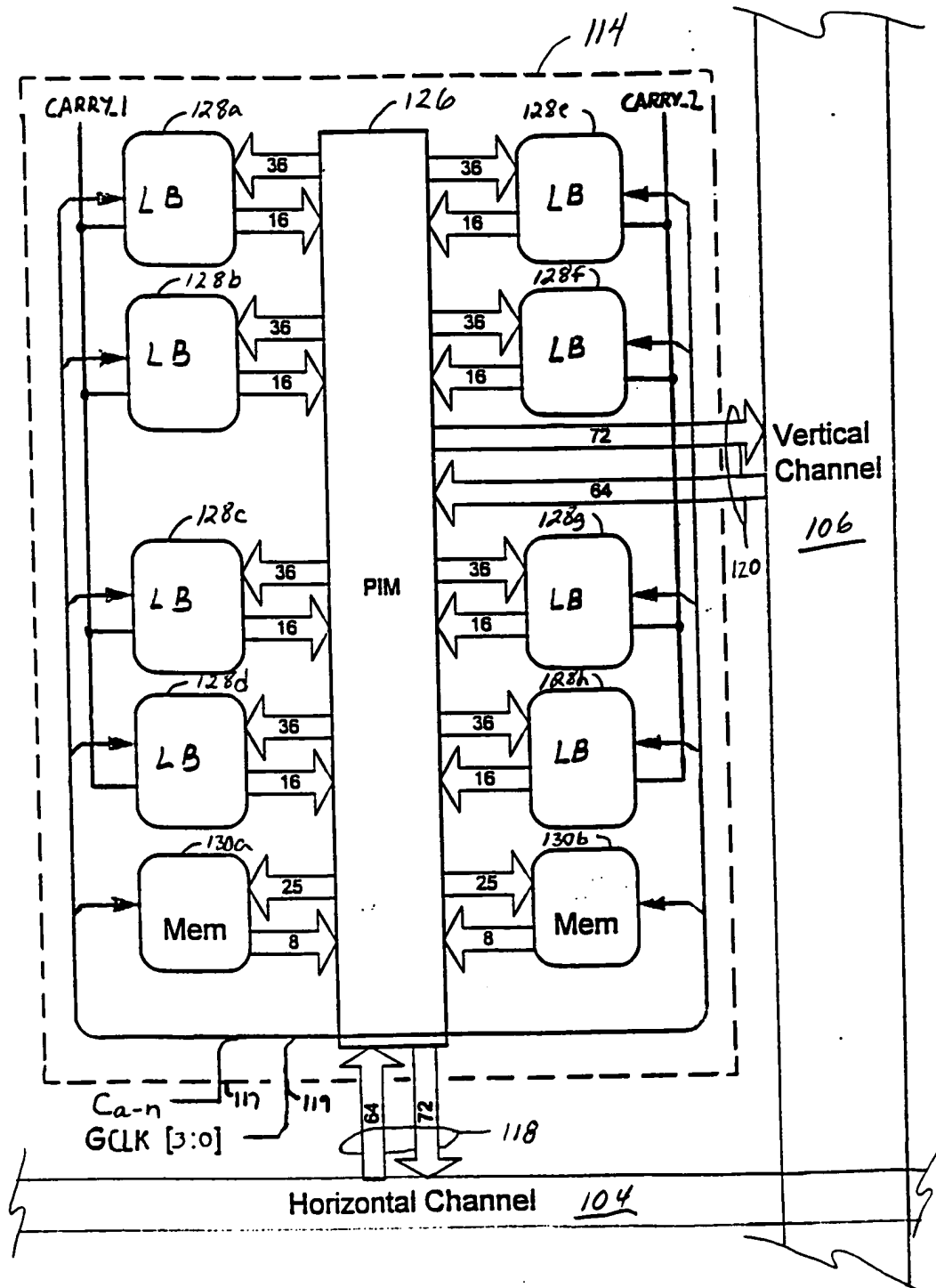


FIG.3

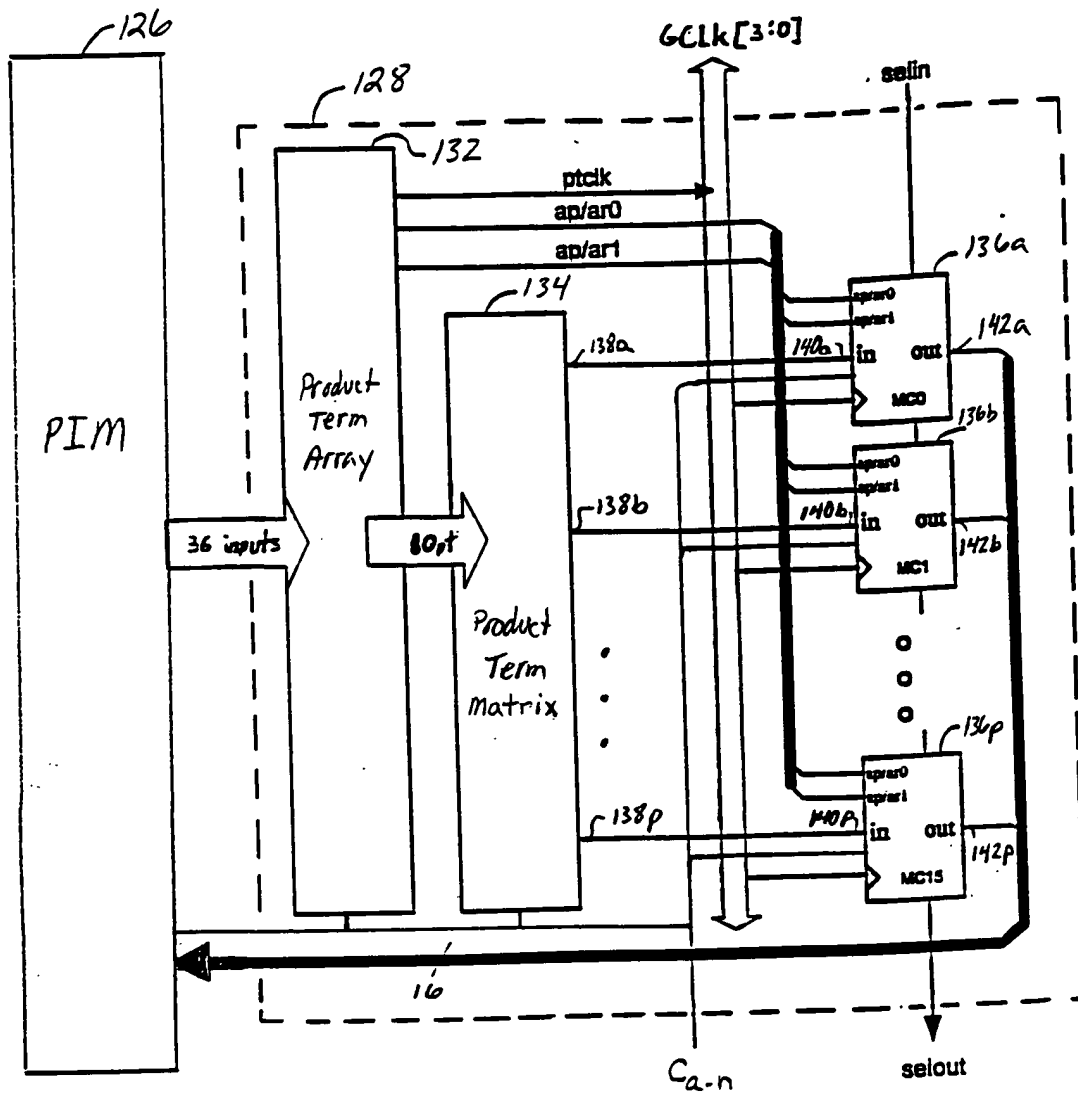
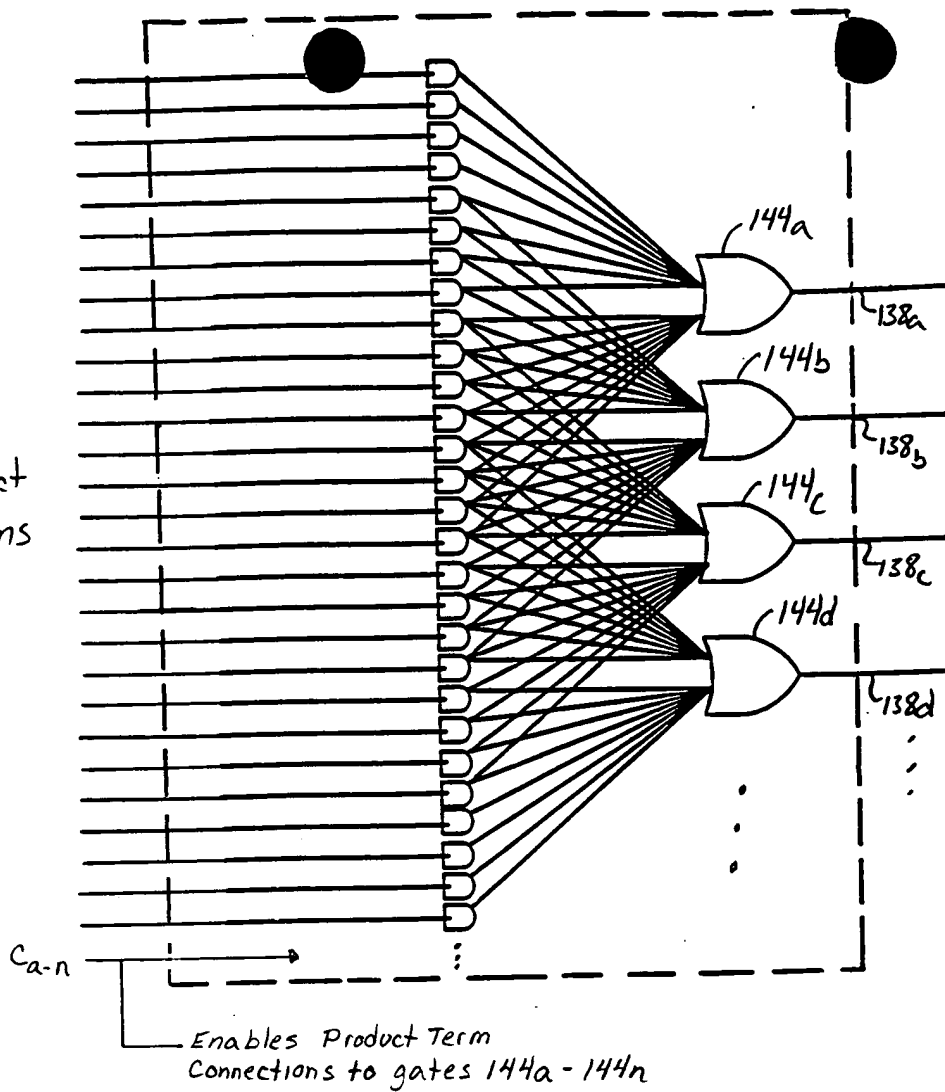


FIG.4

Product
Terms



To
Macro cells
136a - 136p

FIG.5

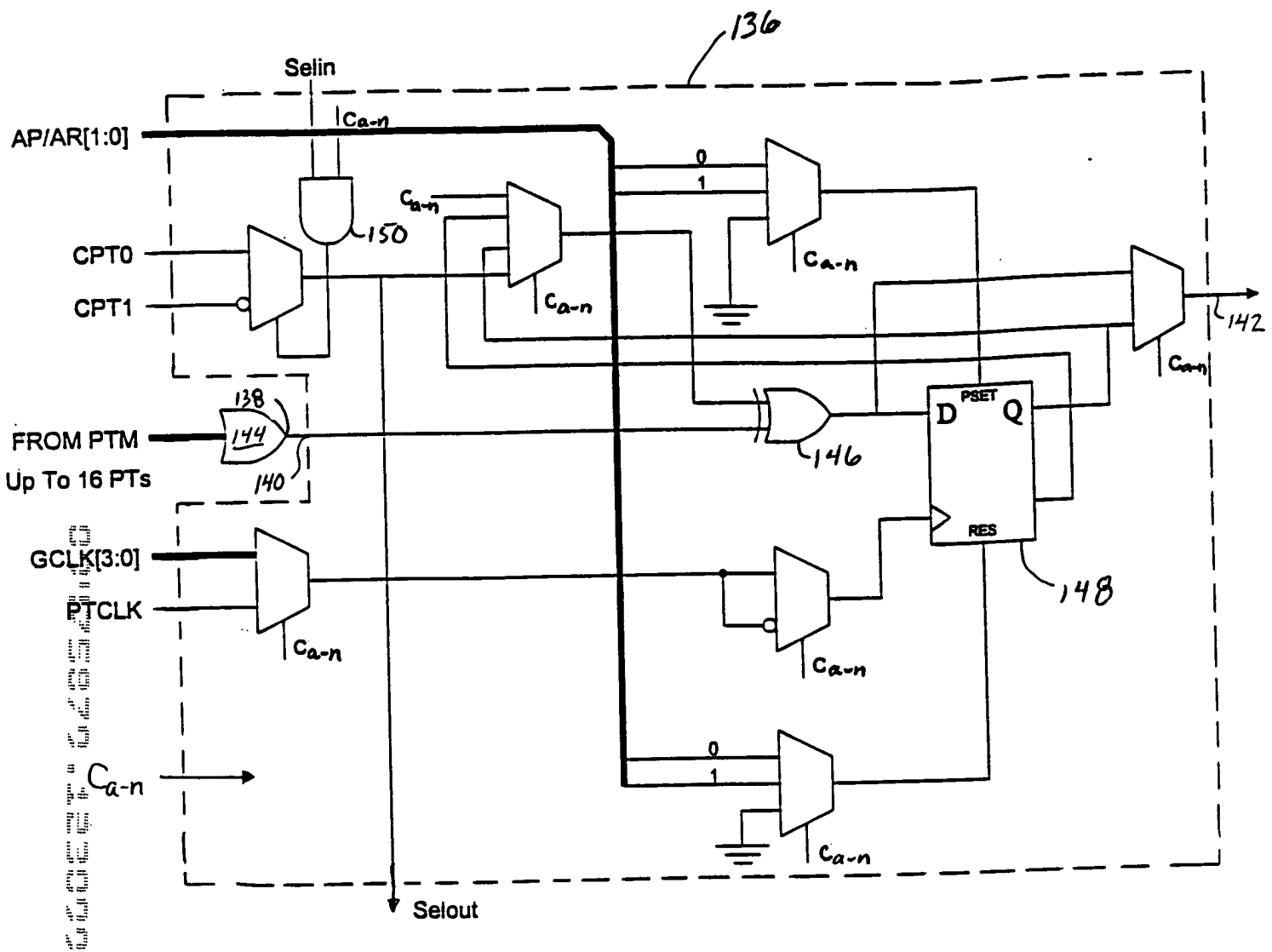


FIG.6

FIG. 7 is a block diagram of a memory array circuit 130, which includes a memory array 152, a write pulse generator 162, and a read pulse generator 168. The circuit is controlled by a global clock signal gclk[3:0] and a write enable signal we. The memory array 152 is connected to a data input din[7:0] and a data output dout[7:0]. The read pulse generator 168 is connected to the memory array 152 and a read enable signal rst. The write pulse generator 162 is connected to the memory array 152 and a write enable signal we. The circuit also includes a power down block 180 and a clock divider 172. The clock divider 172 is connected to the global clock signal gclk[3:0] and a clock output signal outclk. The power down block 180 is connected to the memory array 152 and a power down signal Ca-n. The circuit is shown in a perspective view with a top surface and a bottom surface.

130

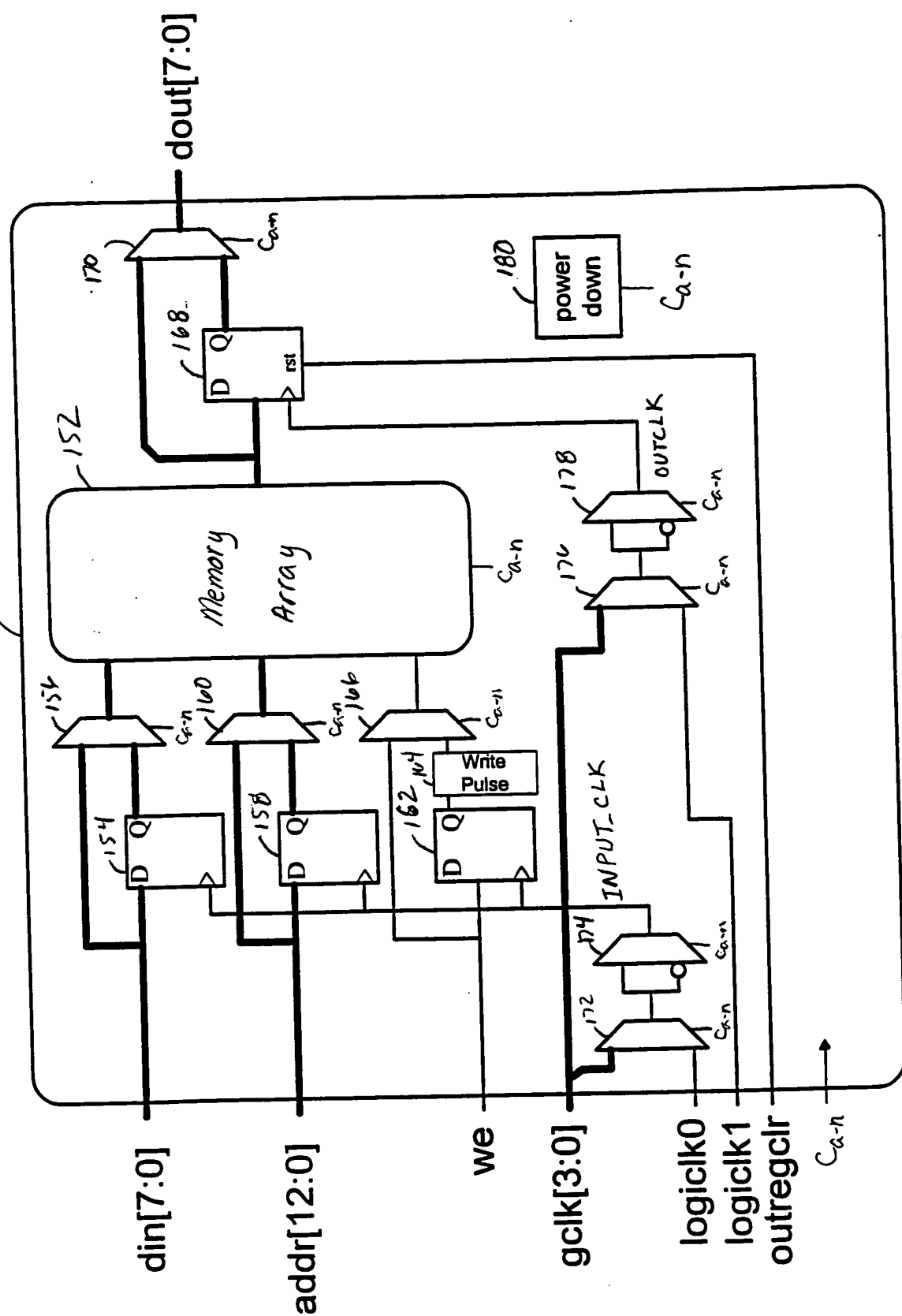


FIG. 7

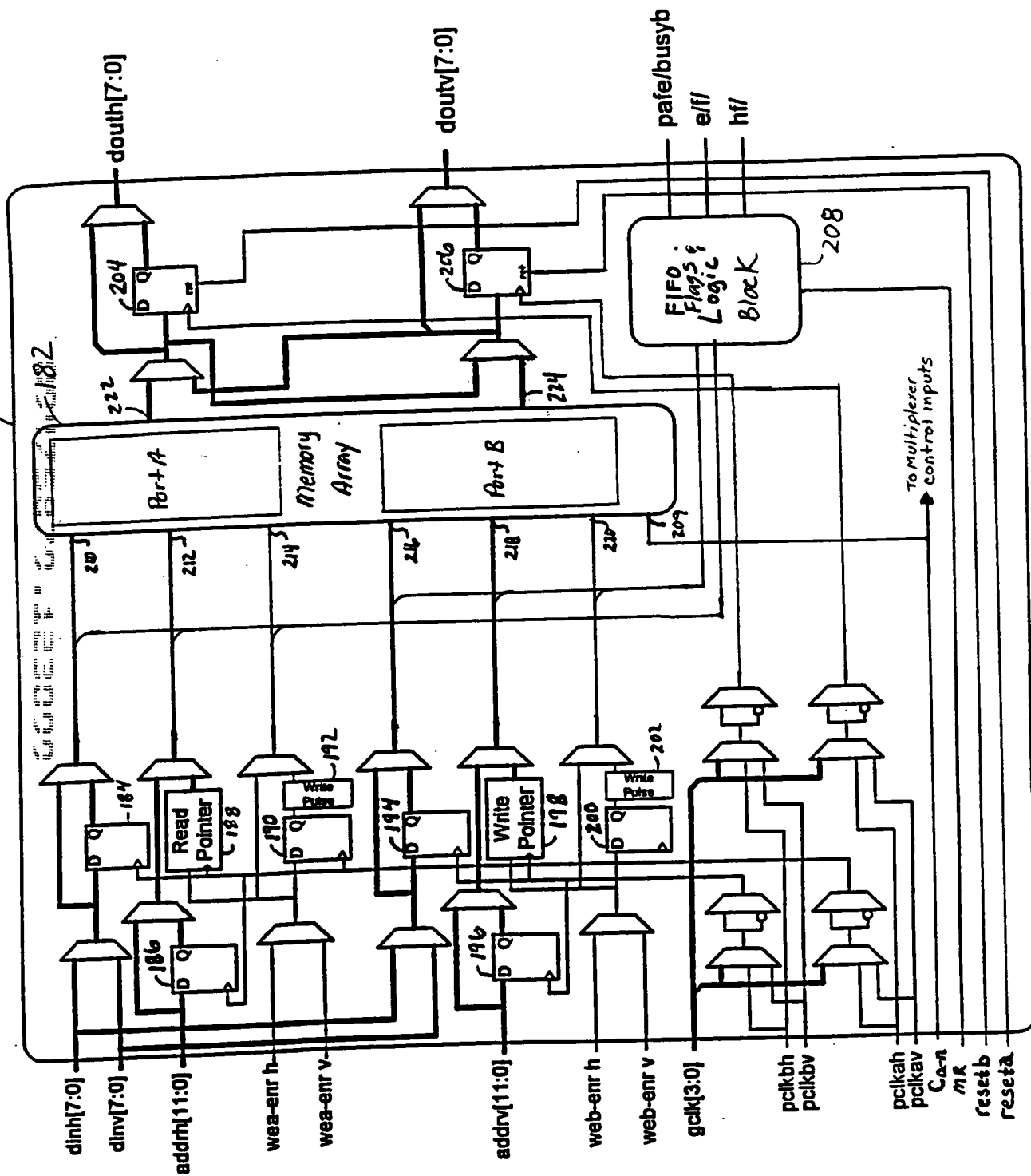


FIG. 8

116

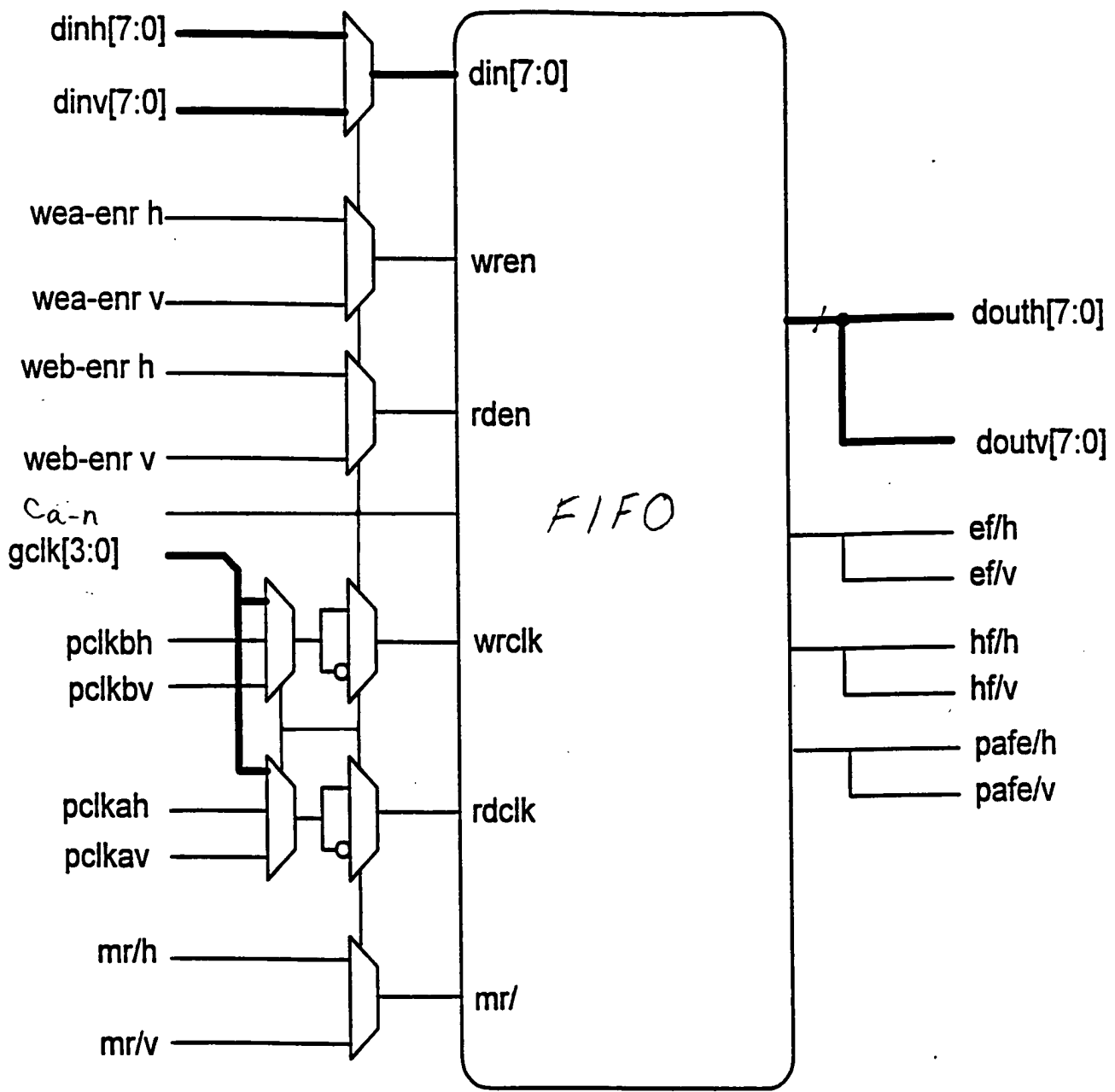


FIG.9

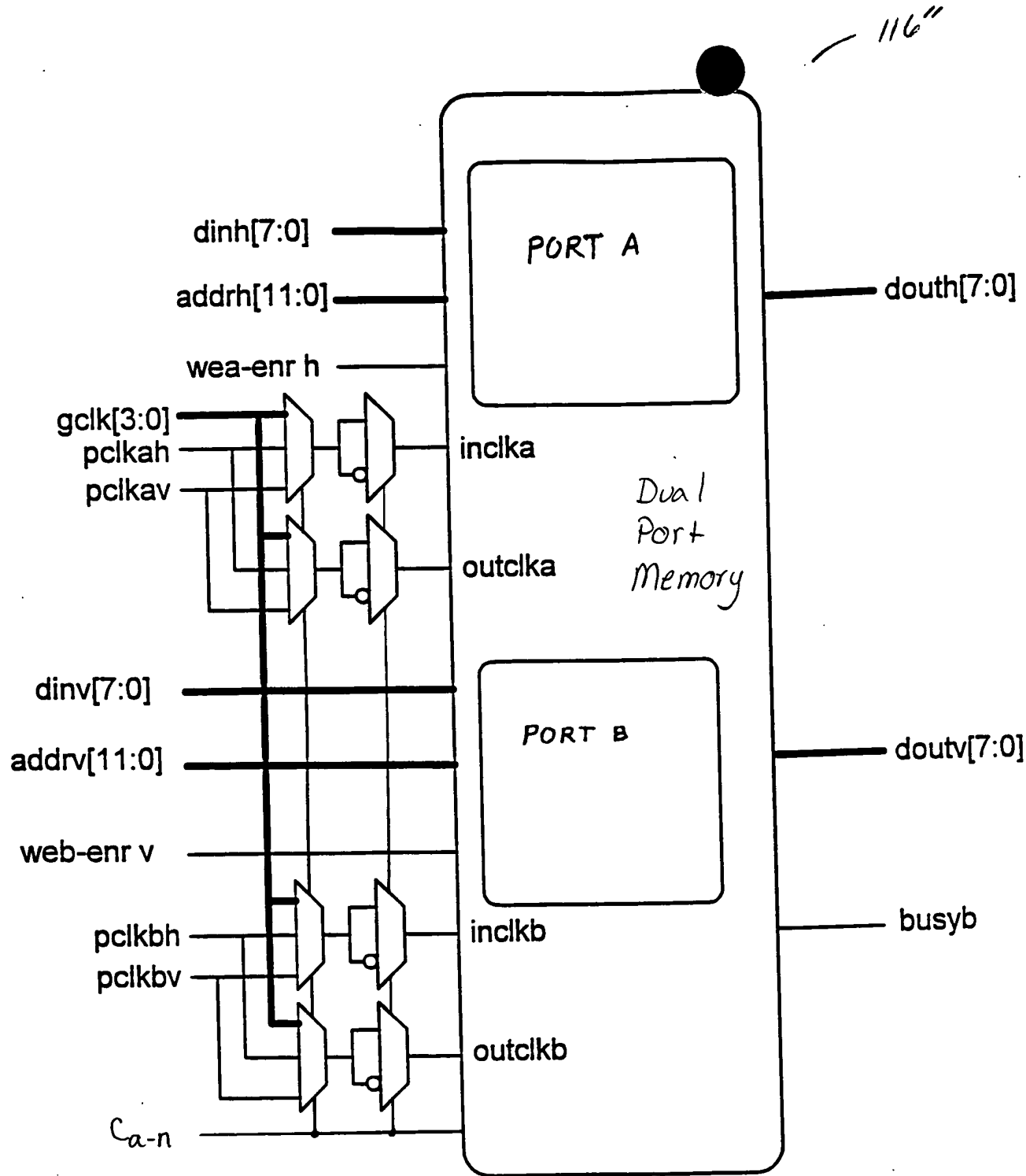


FIG.10

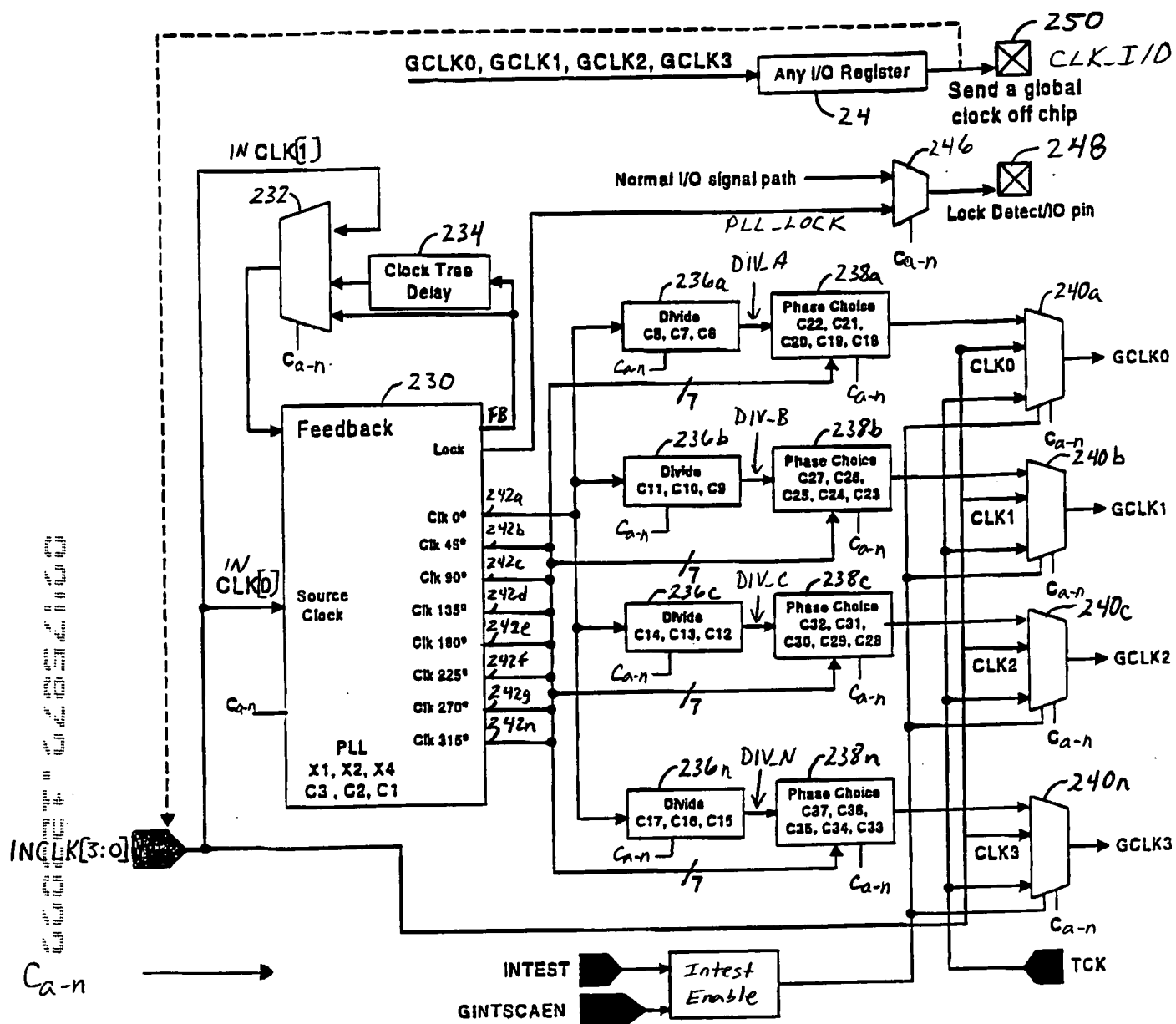


FIG.11

FIG. 12 is a block diagram of a system 100, including a processor 102, a memory 104, and an I/O device 106. The processor 102 is connected to the memory 104 and the I/O device 106. The memory 104 is connected to the processor 102 and the I/O device 106. The I/O device 106 is connected to the processor 102 and the memory 104.

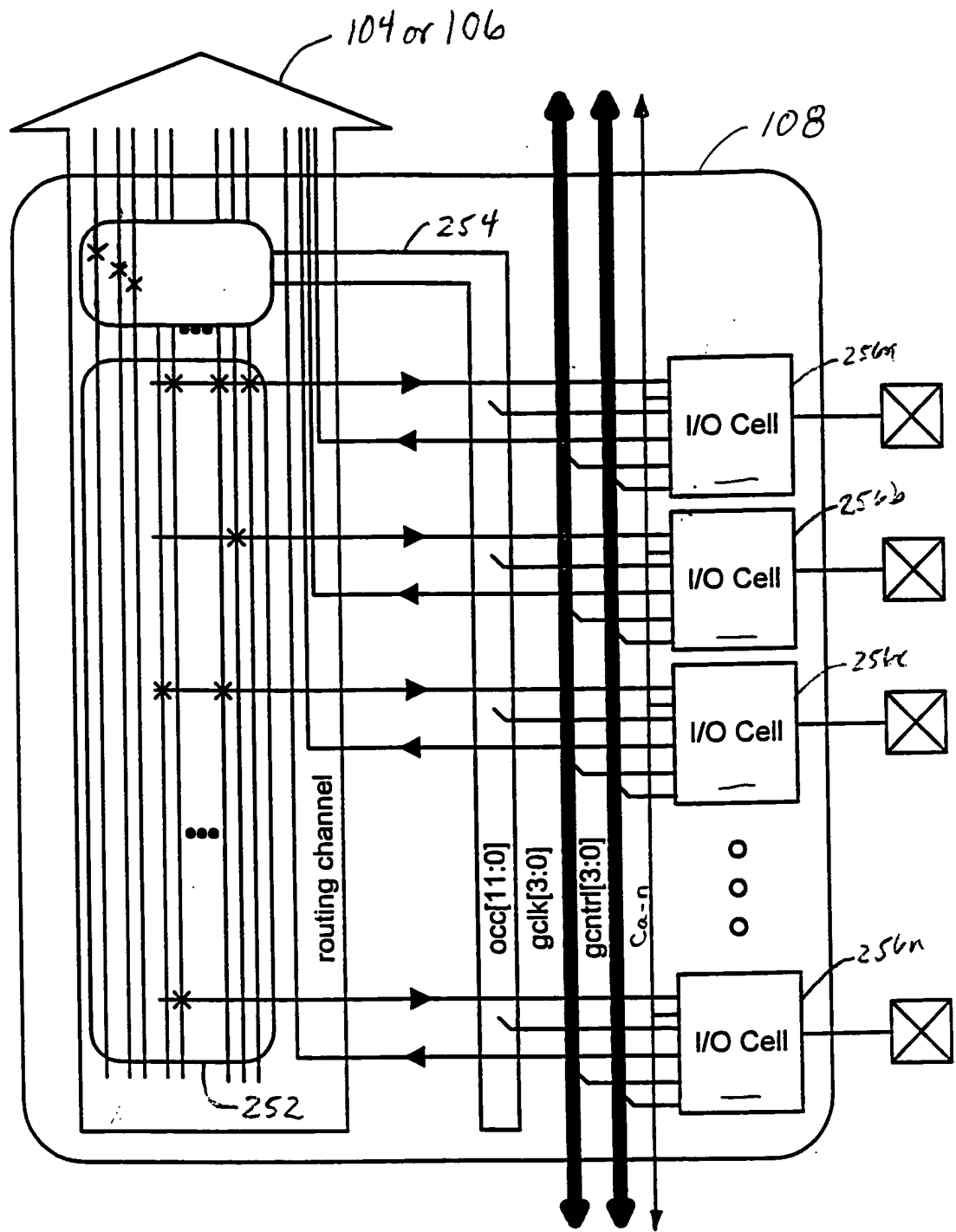


FIG.12

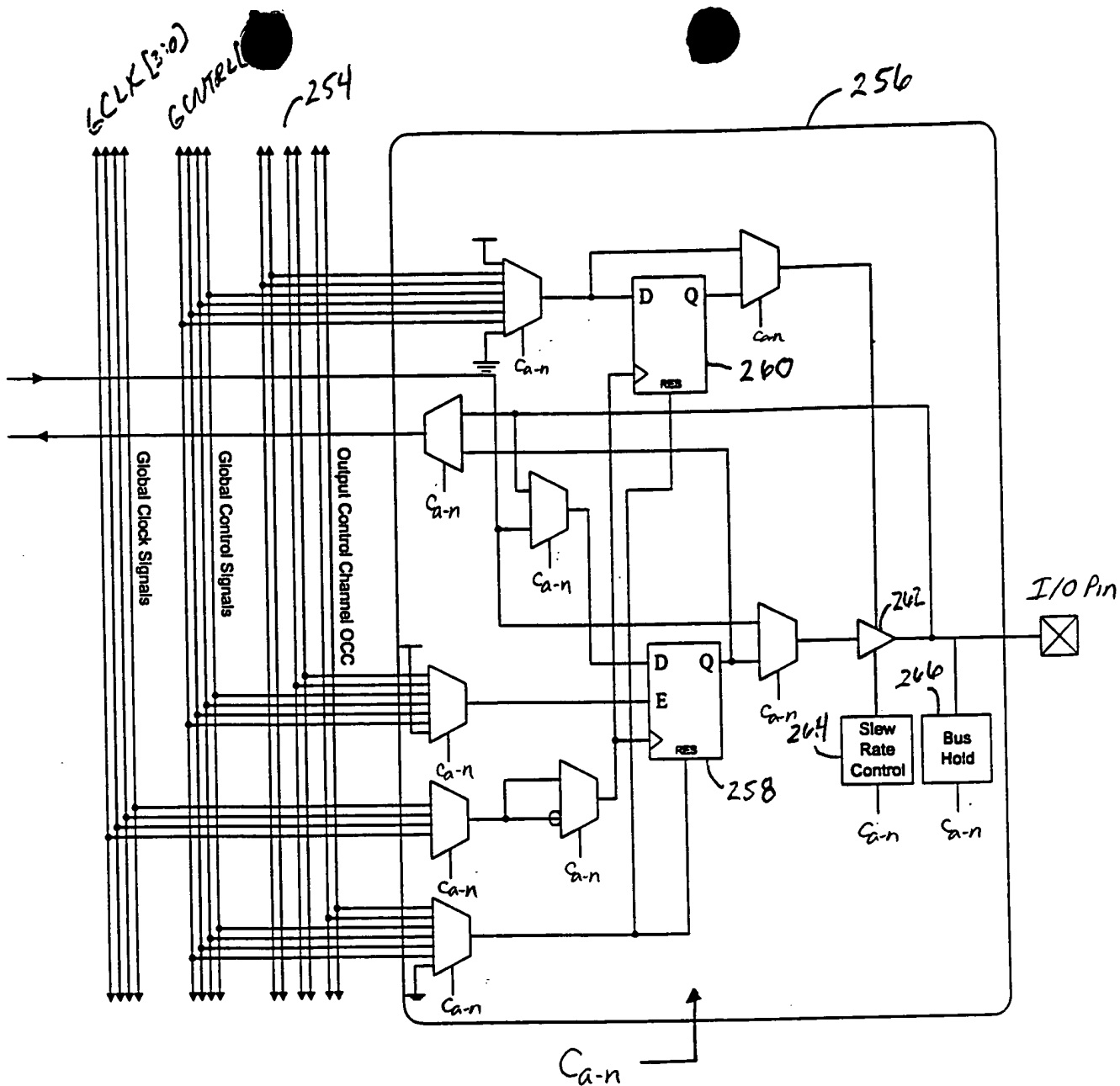


FIG.13

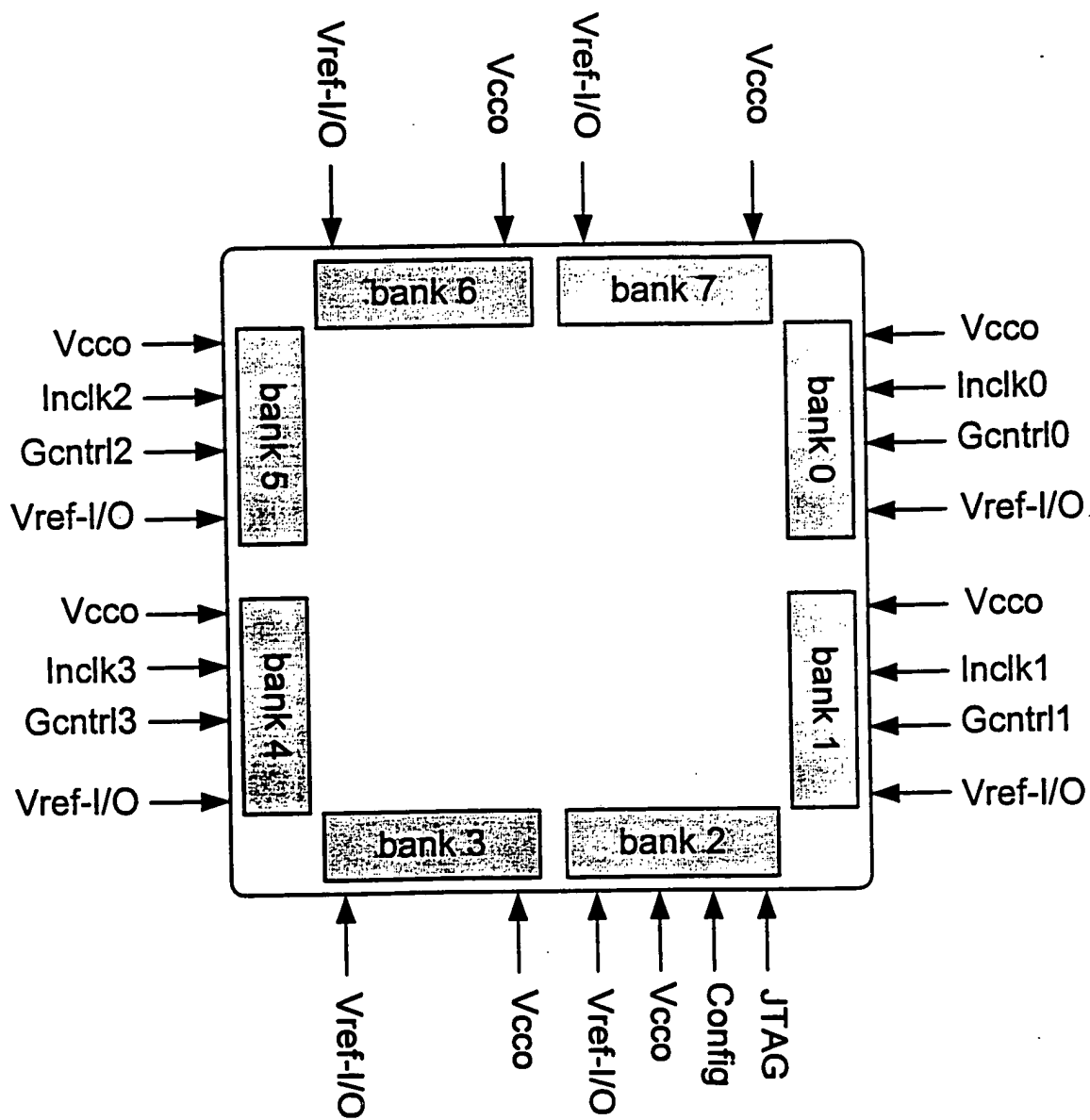


FIG.14